

Verifying Parameterized Networks

Specified by

Vertex-Replacement Graph Grammars

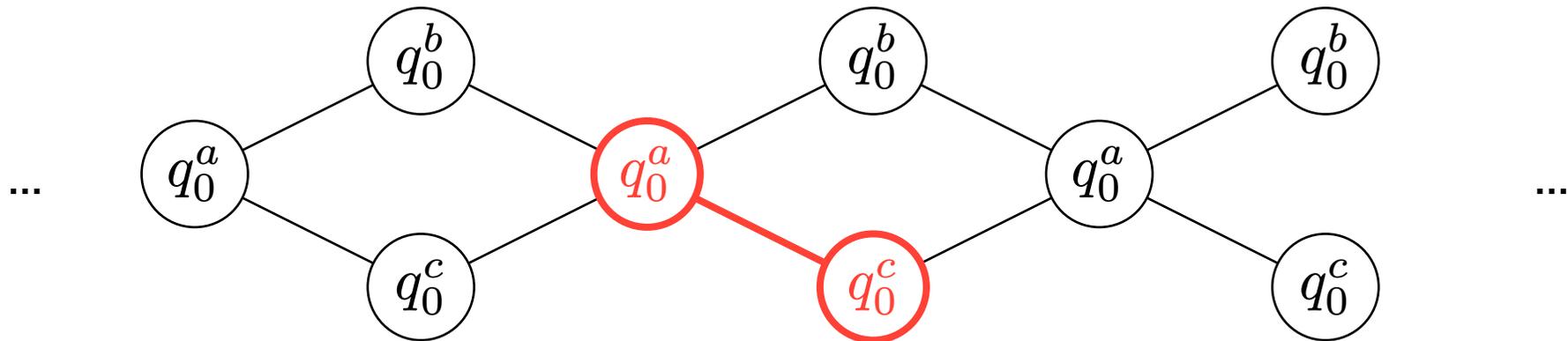
Neven Villani, Radu Iosif, Arnaud Sangnier

Univ. Grenoble Alpes, Verimag

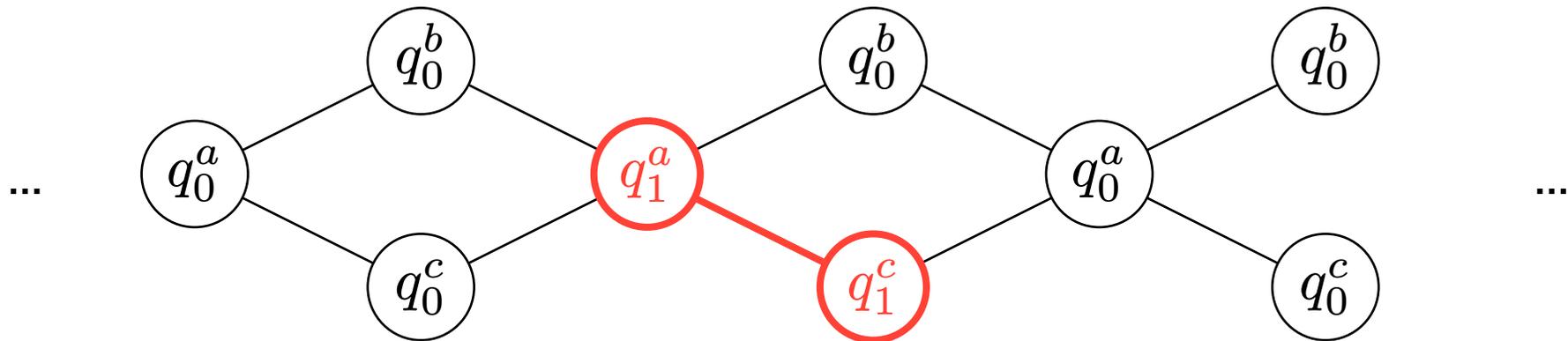
2025-05-21; NETYS (Rabat)

Context

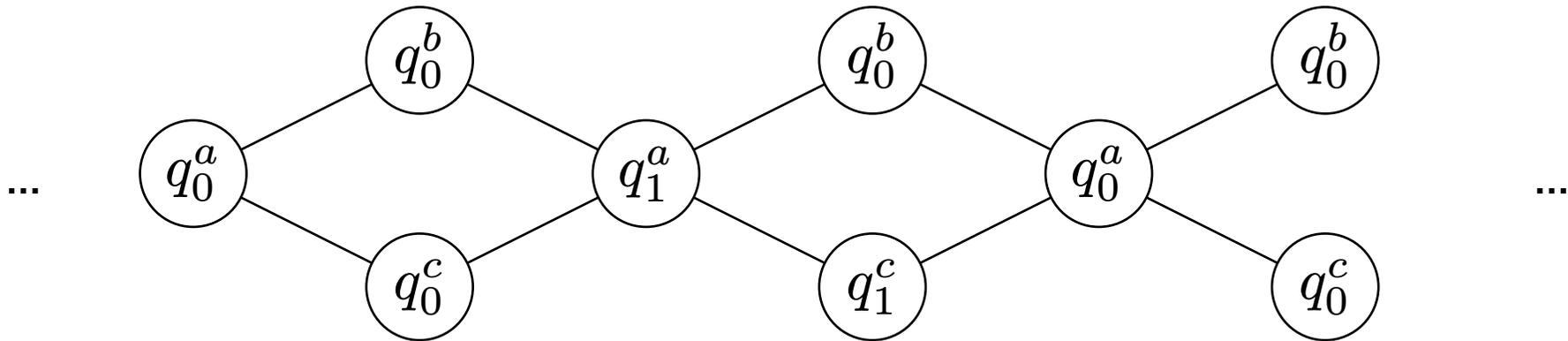
- Parameterized structured networks
- Non-homogeneous
- Binary rendezvous
- Locally finite memory
- Safety properties



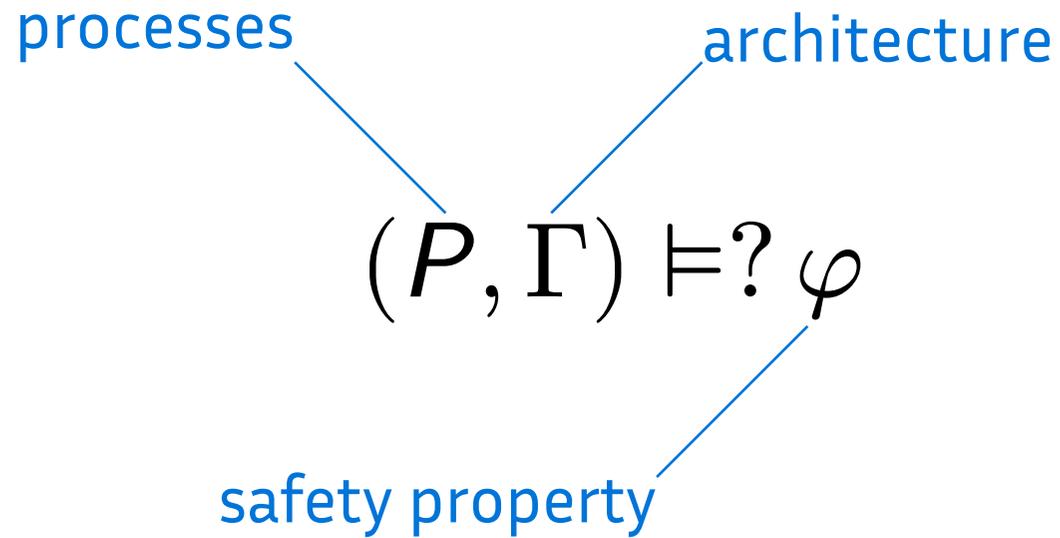
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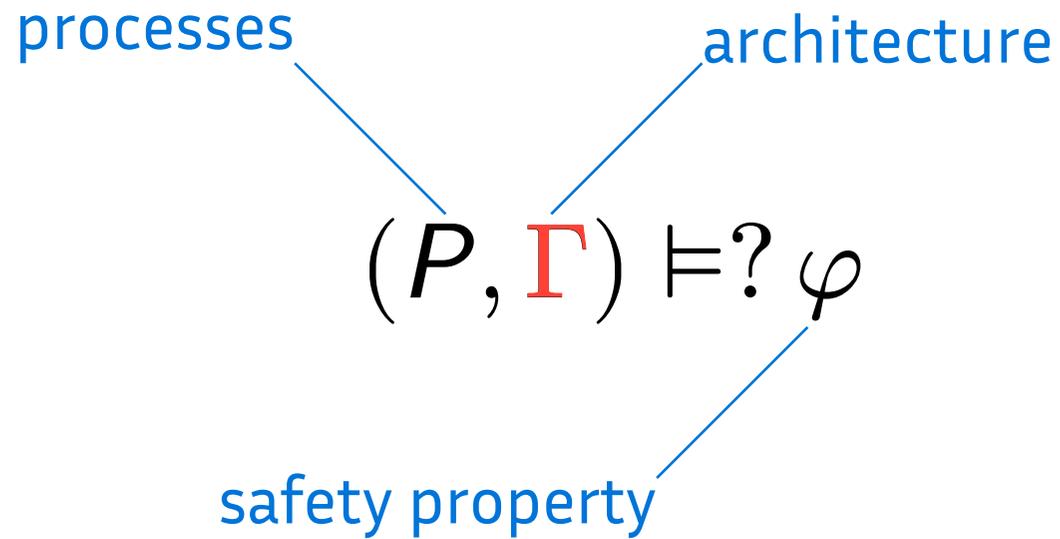


- Parameterized structured networks
- Non-homogeneous
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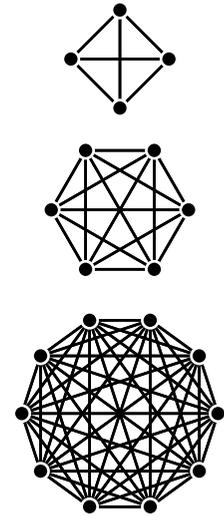
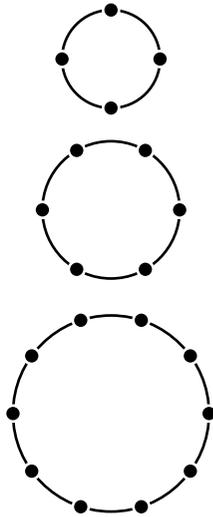
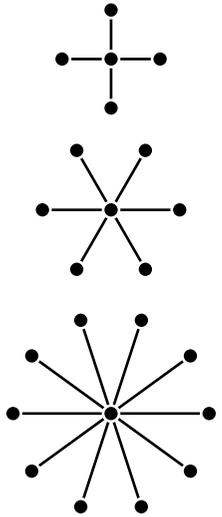
$\#q_1^b > 1 \wedge \#q_1^c > 1$ reachable ?



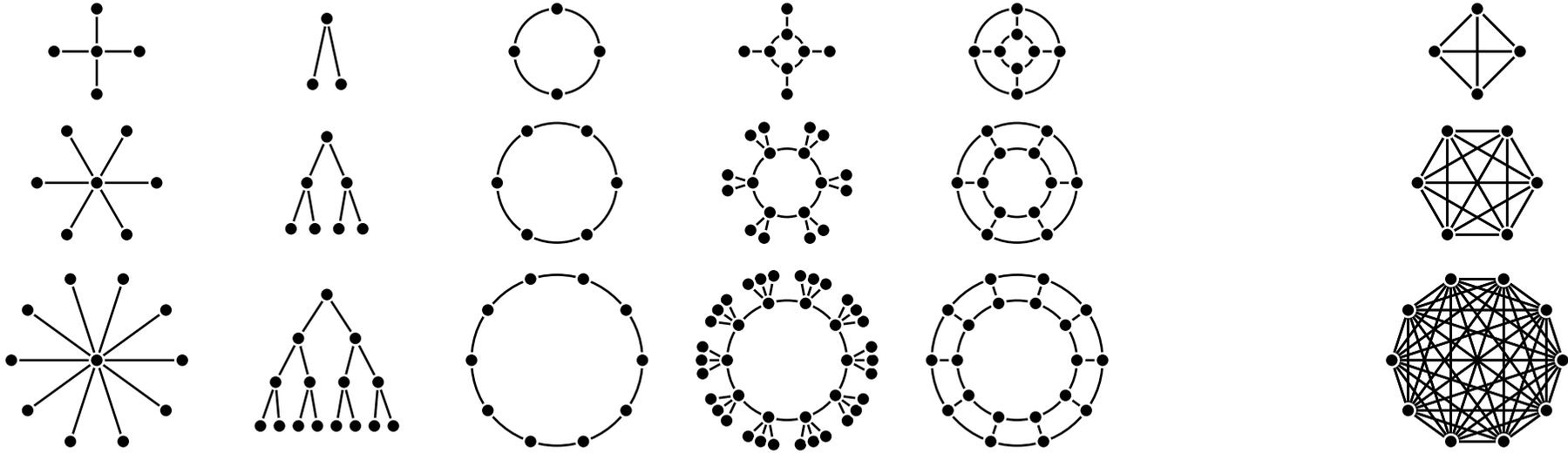


What formalism to describe architectures ?

Context



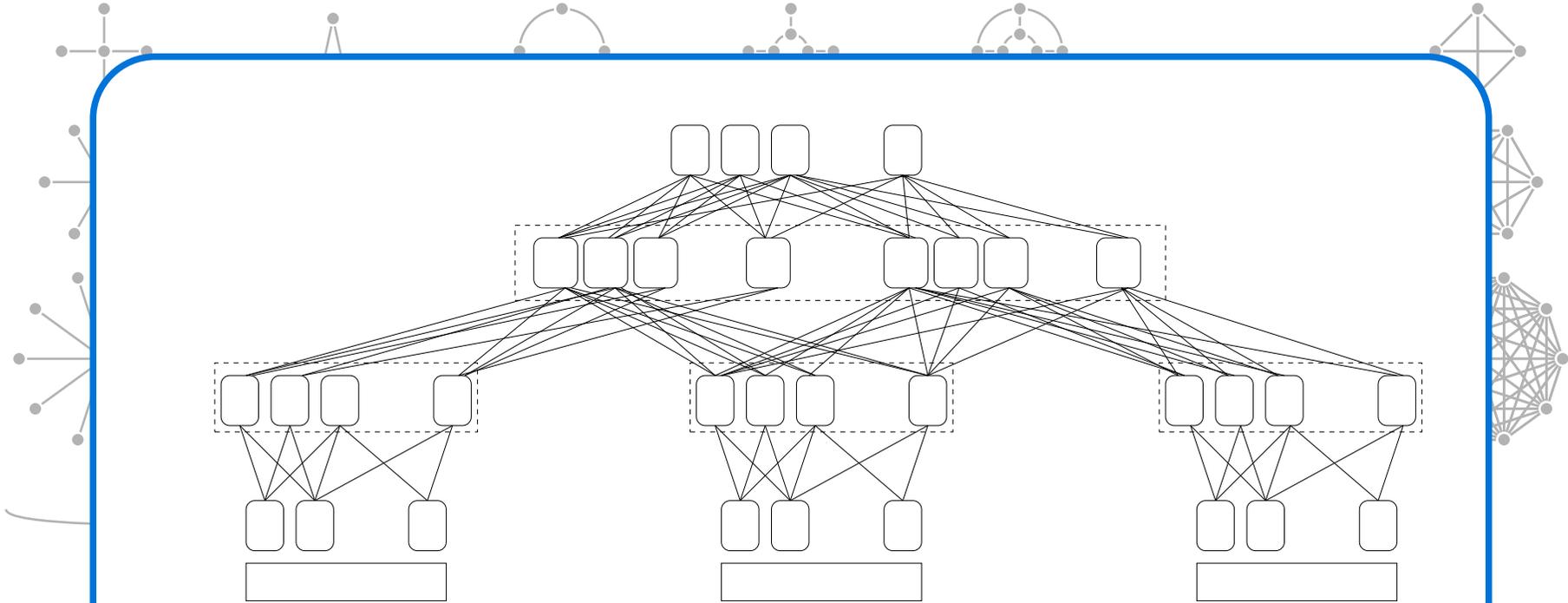
What formalism to describe architectures ?



Hyperedge **R**eplacement (sparse only)

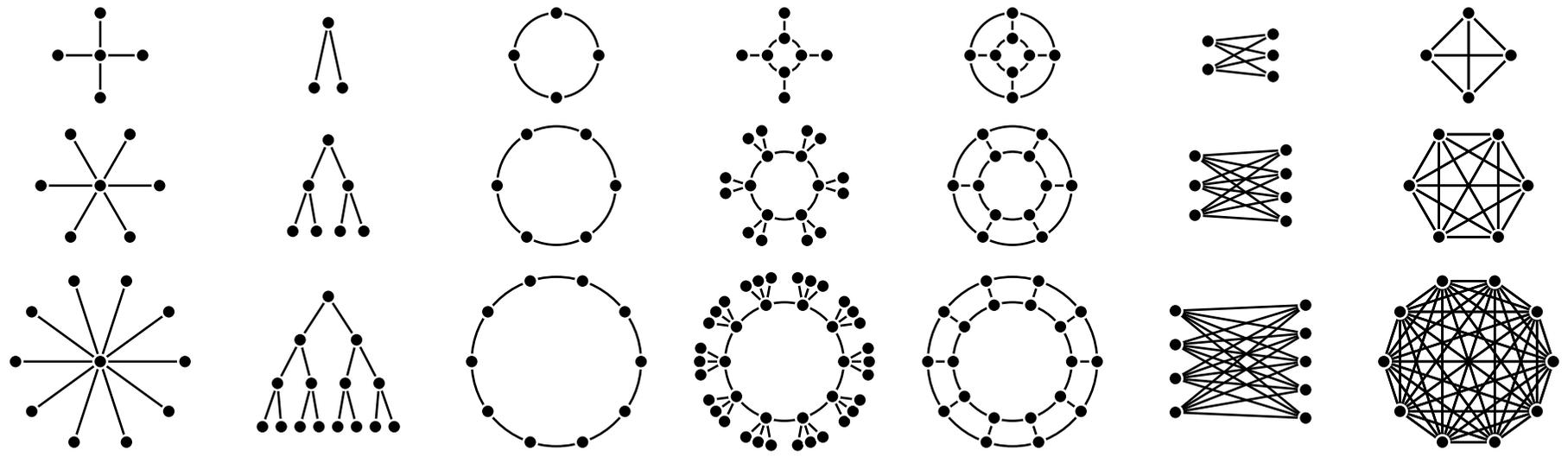
e.g., us, VDS 2025 + CAV 2025

What formalism to describe architectures ?



Azure Datacenter Topology
Greenberg et al., SIGCOMM 2009

What formalism to describe architectures ?



Hyperedge **R**eplacement (sparse only)
e.g., us, VDS 2025 + CAV 2025

Vertex **R**eplacement (incl. some dense)

A **translation** from VR to HR architectures.

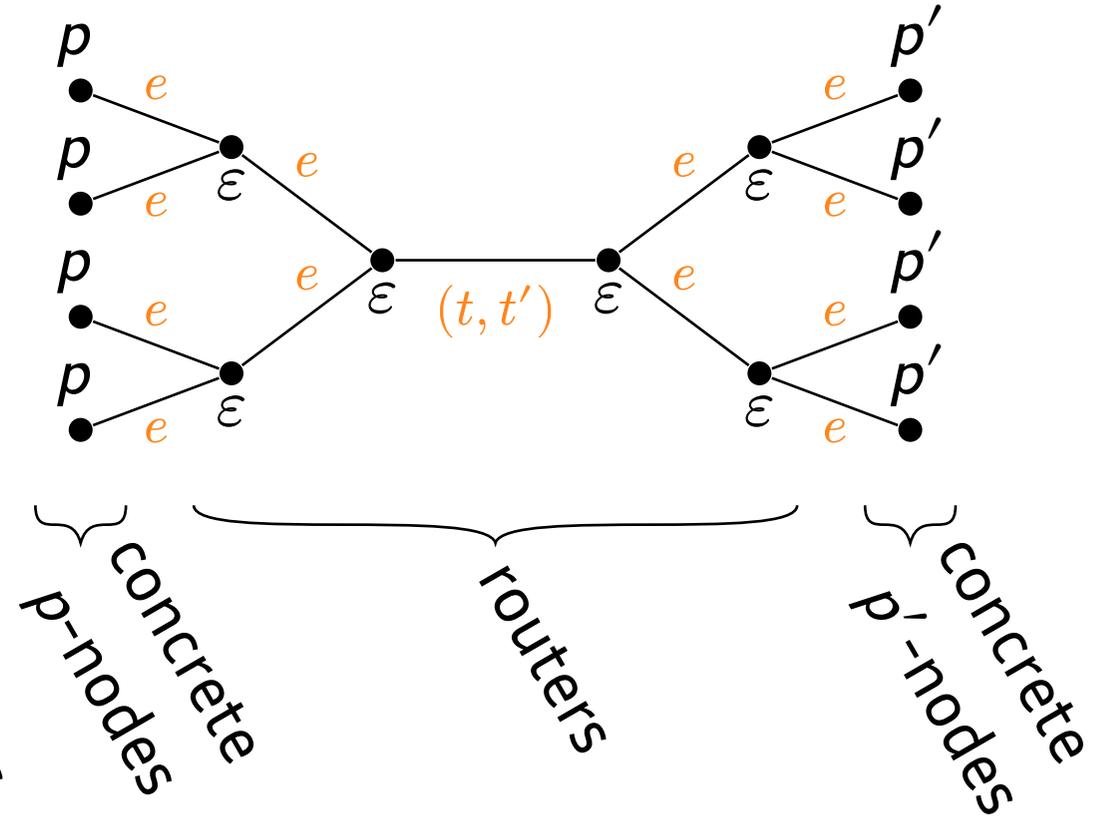
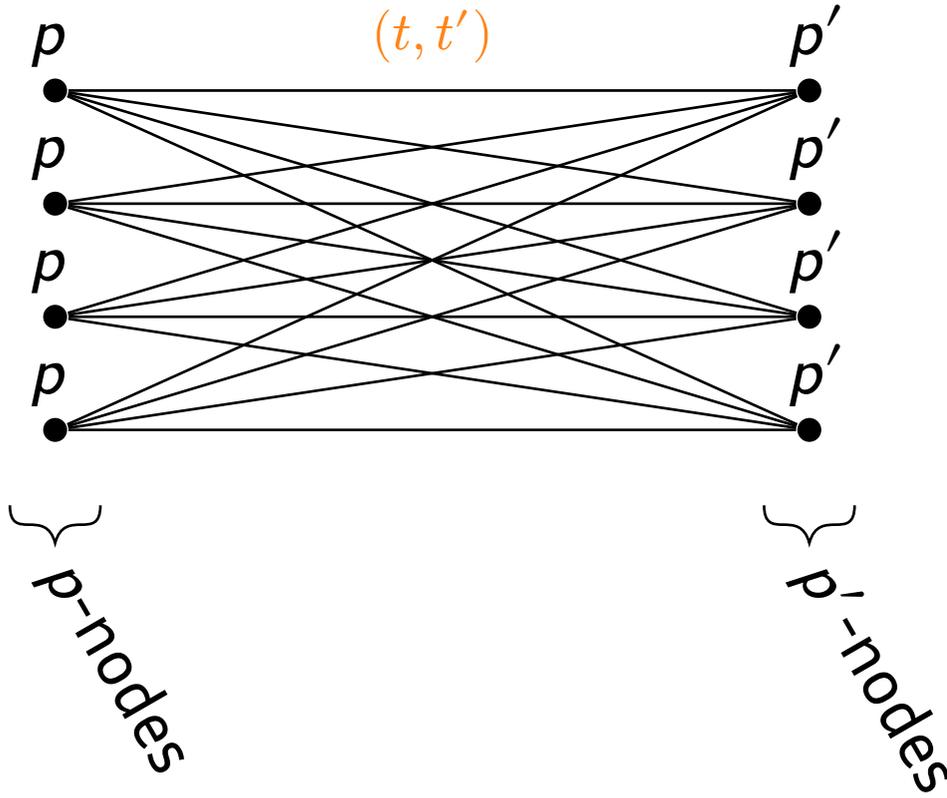
Adapting a translation from VR to HR architectures **to the case of systems**, and studying which safety properties are preserved.

B. Courcelle, Structural Properties of Context-Free Sets of Graphs Generated by Vertex Replacement, *Information and Computation*, 1995

Key idea

(t, t')
→

$e^* (t, t') e^*$
⋈ → ⋈

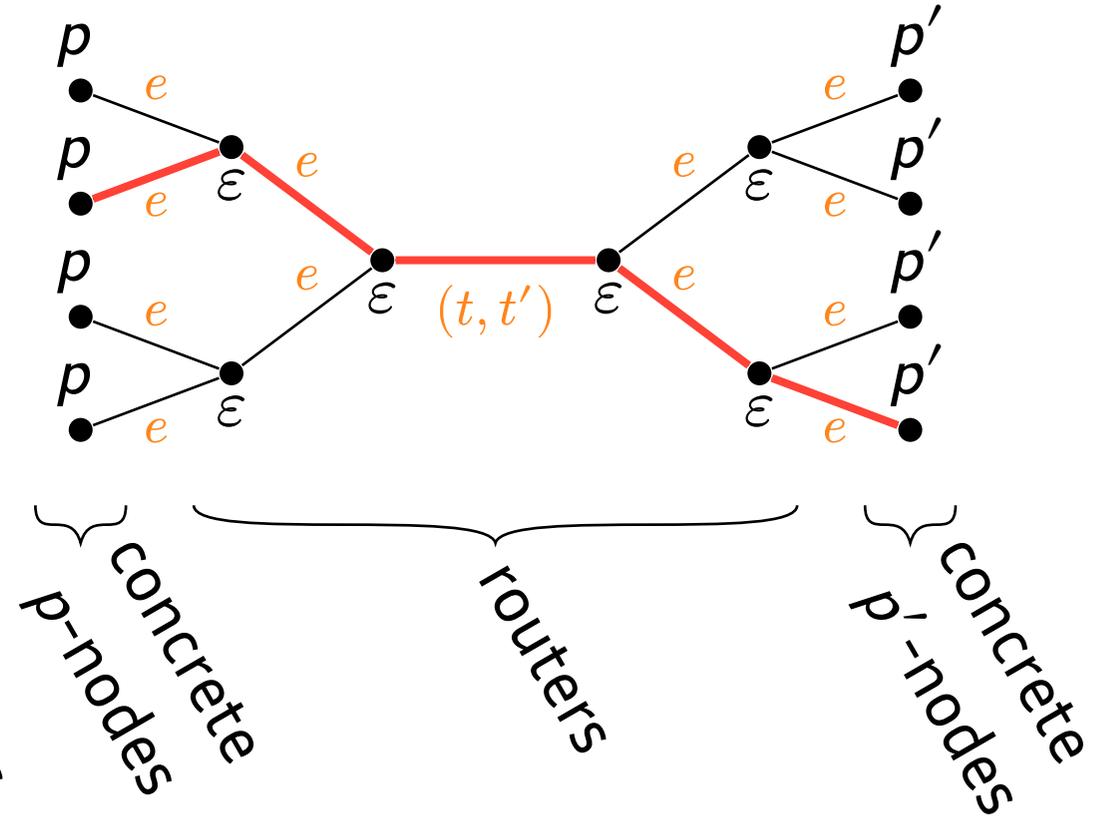
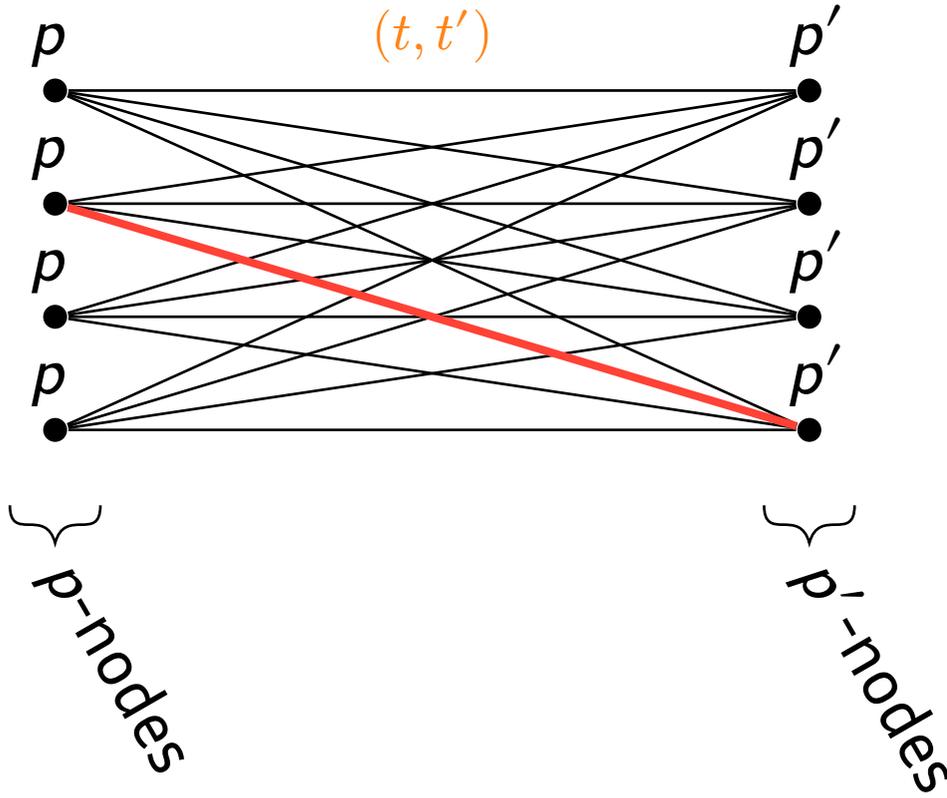


Key idea

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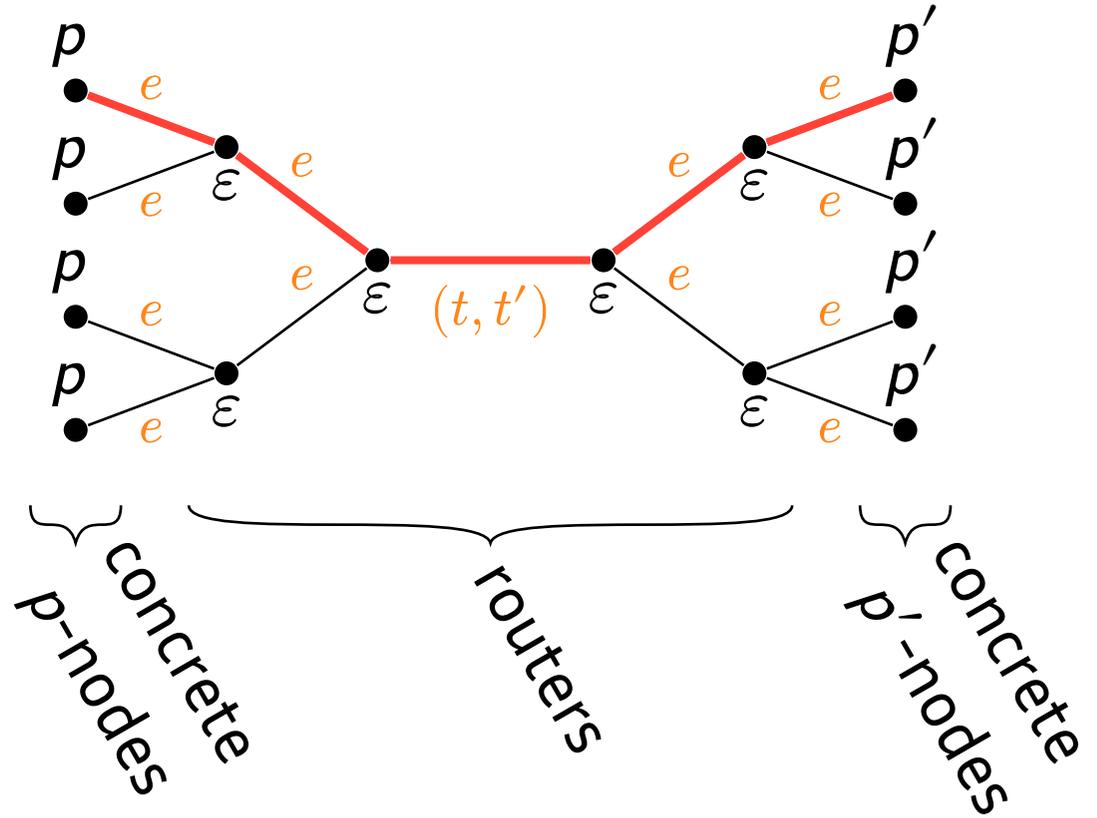
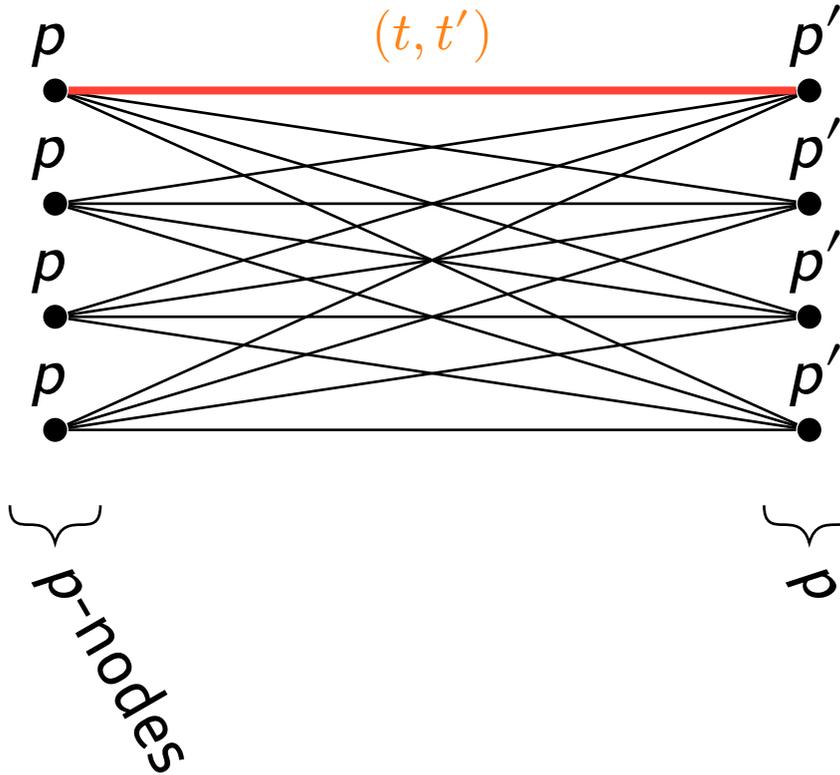


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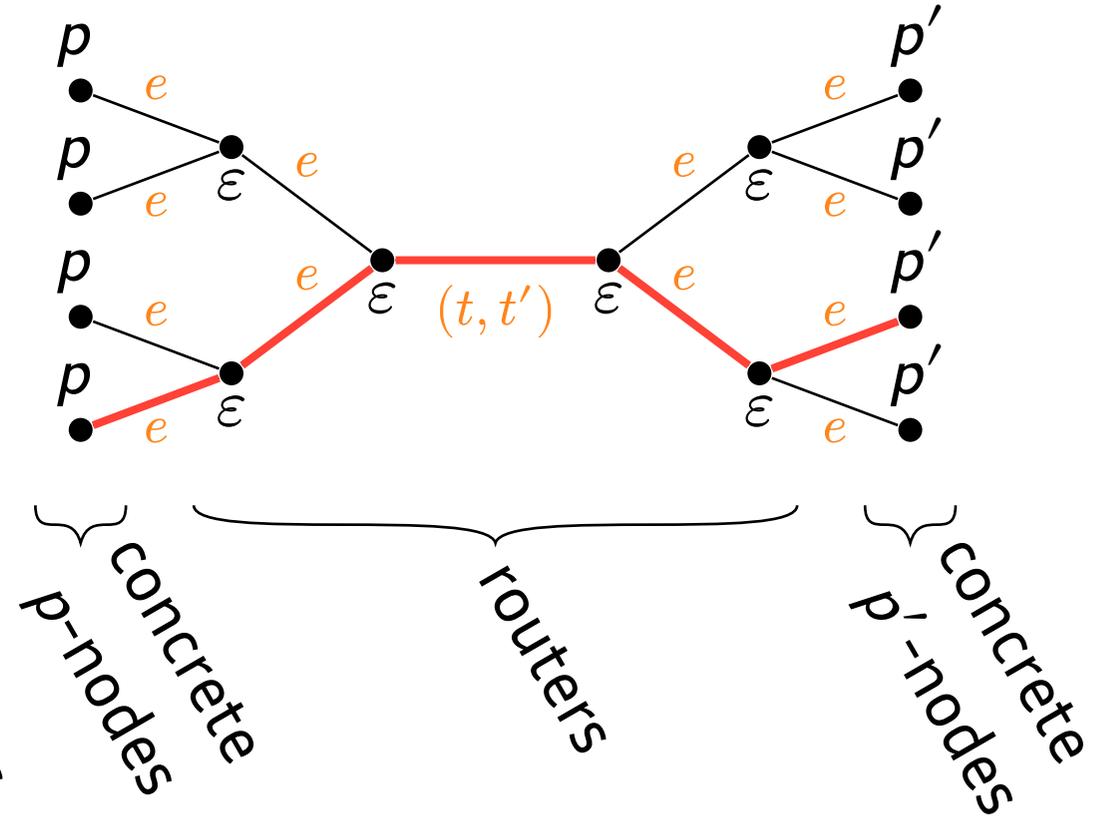
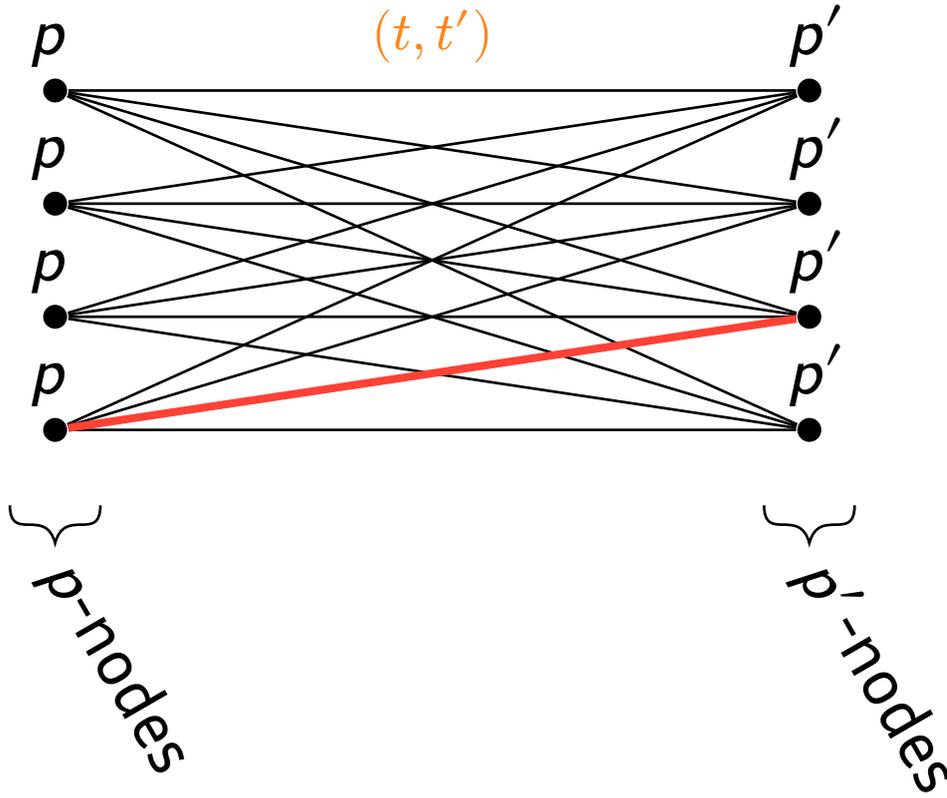
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Key idea

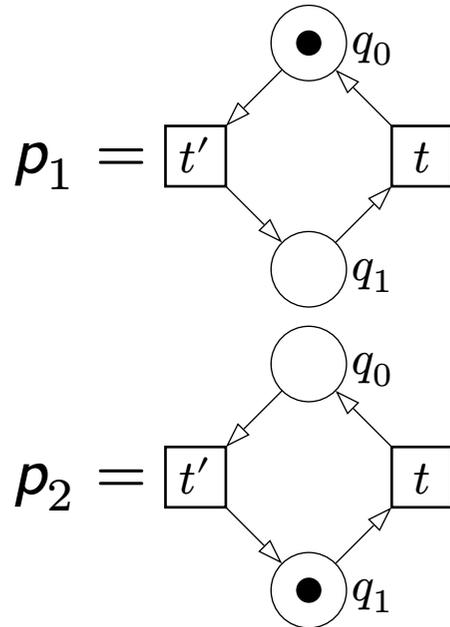
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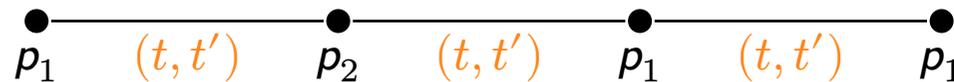
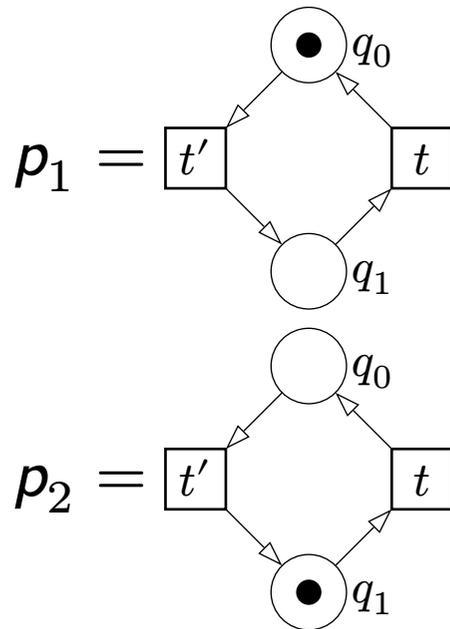


Encoding of Networks

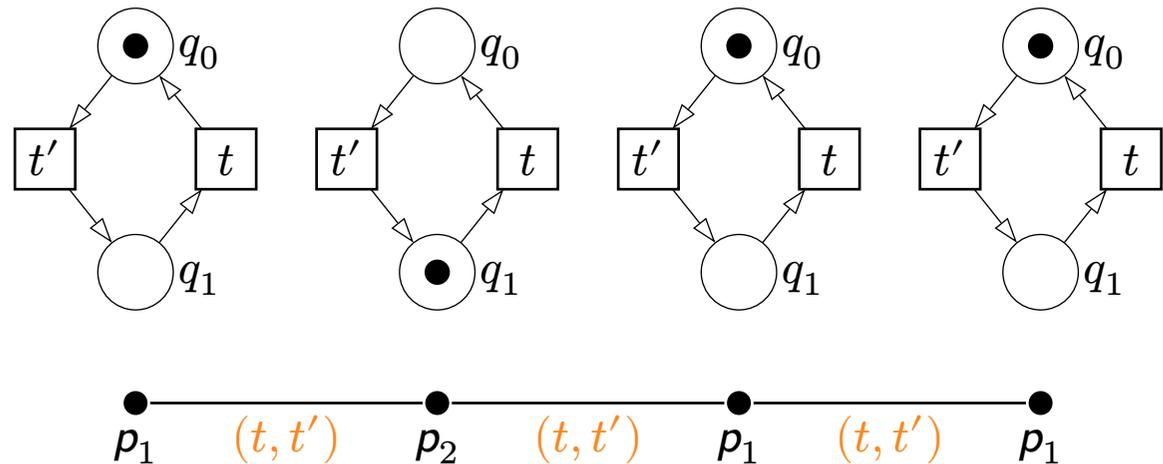
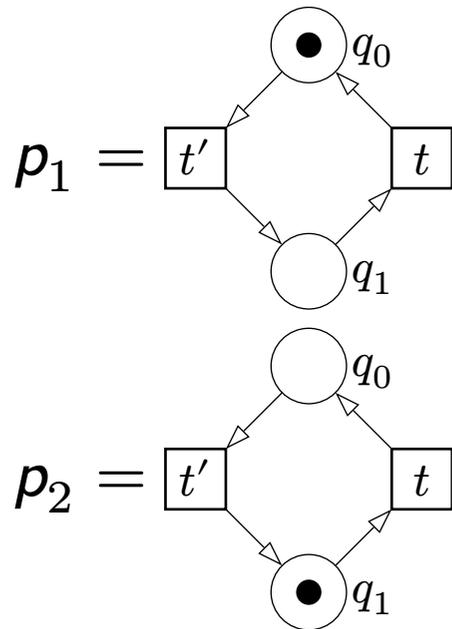
- process types p_1, p_2, \dots = Petri nets (PN) with observable transitions



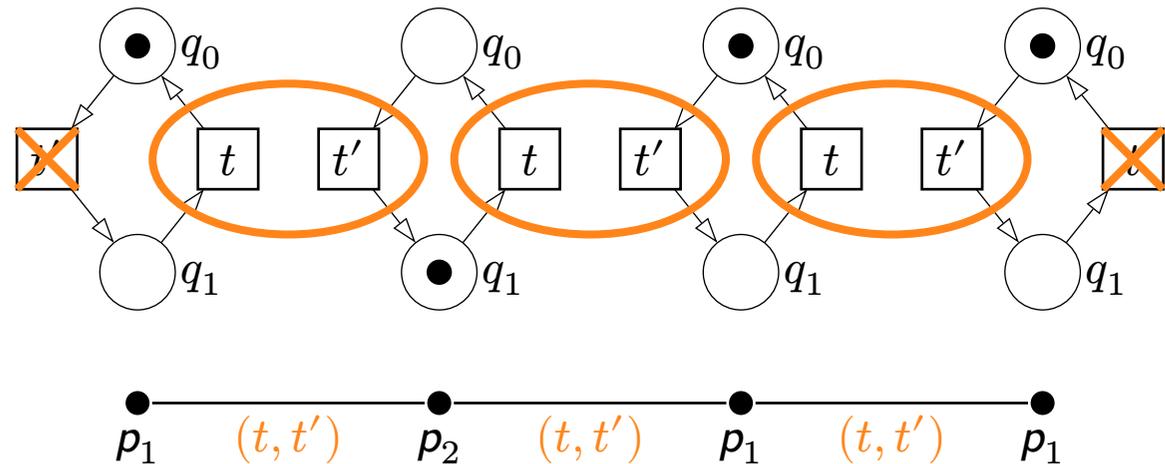
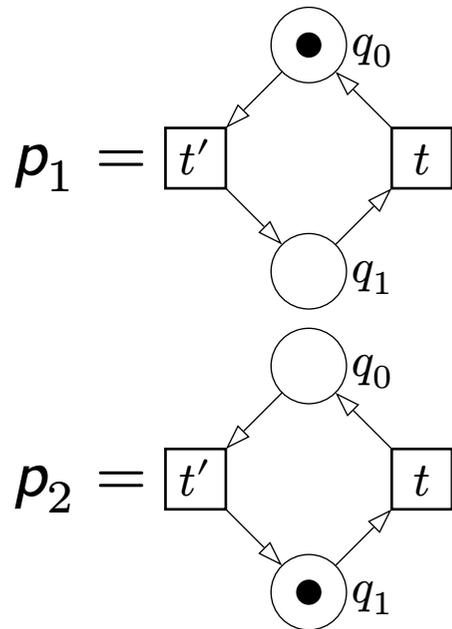
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- system: graph with
 - vertices labeled by a process type
 - edges labeled by pairs of observable transitions



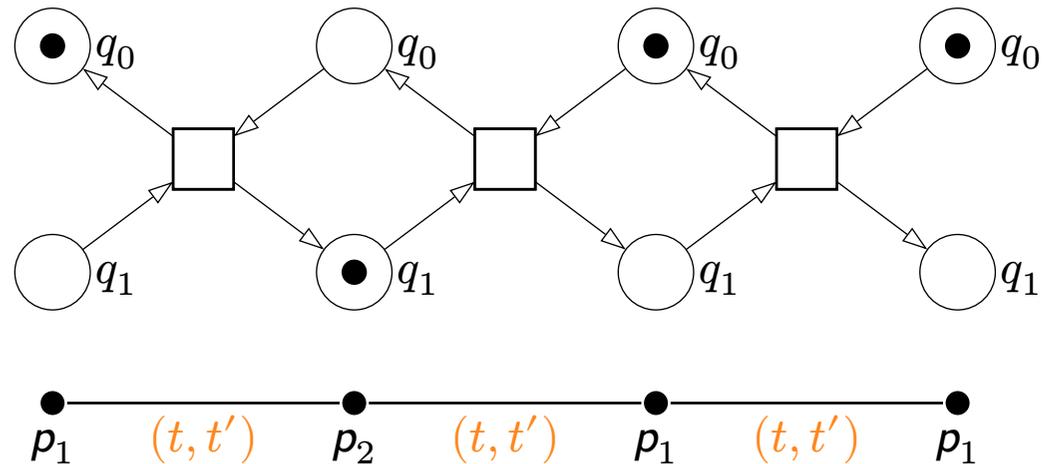
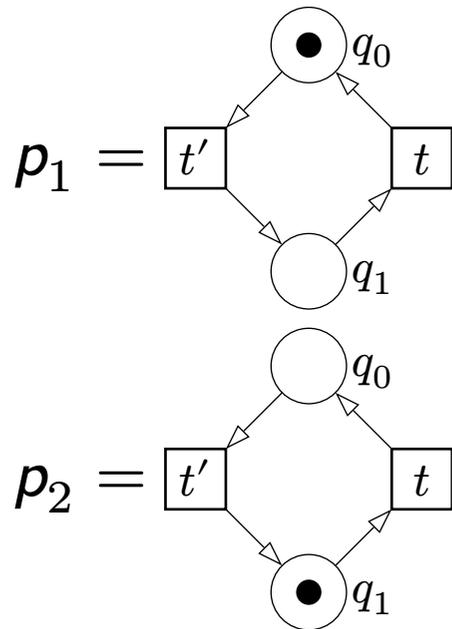
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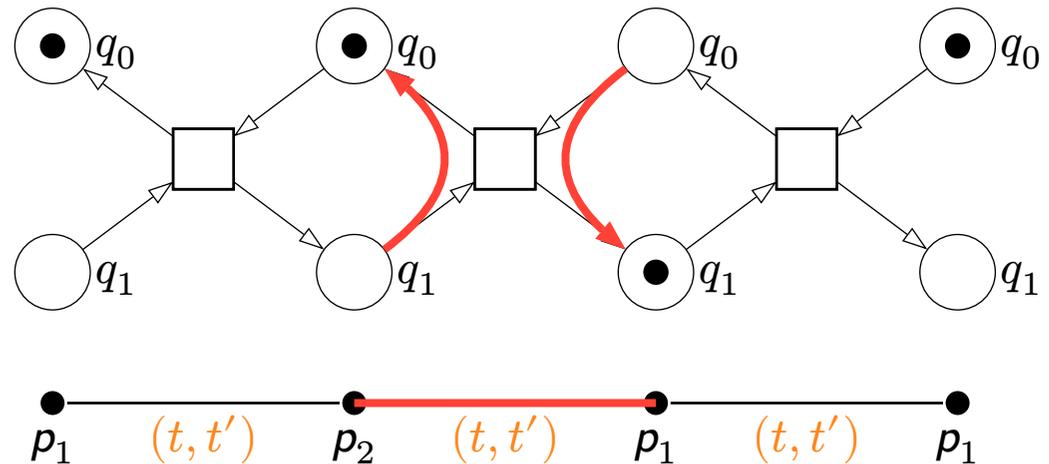
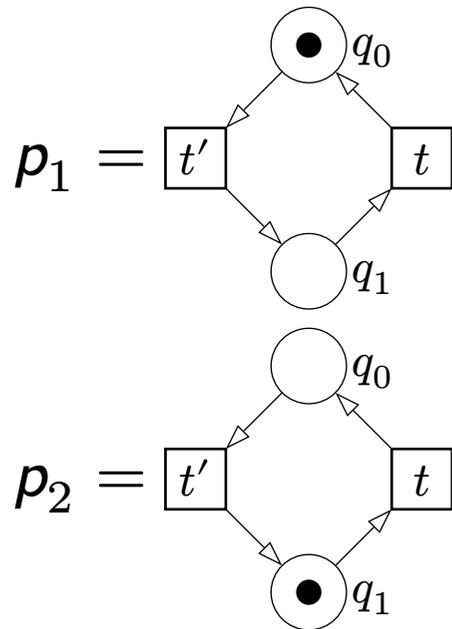
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$\#q^p$ total number of tokens in place q of processes of type p .

α any arithmetic formula on $\{\#q^p \mid q, p\}$

φ reachability/coverability/sequence/etc on α

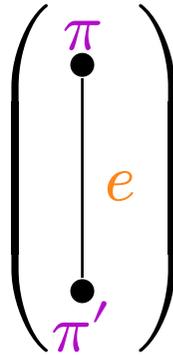
→ interpreted over the firing sequences of the PN

HR & VR

Given by a term in HR/VR.

Context-free grammars generate infinite families of terms,
thus infinite families of architectures.

HR: Single edge

$$\vec{e}_{\pi, \pi'} = \left(\begin{array}{c} \pi \\ \bullet \\ \hline \bullet \\ \pi' \end{array} \right) e$$
The diagram shows a vertical line segment enclosed in large parentheses. At the top of the line is a black dot with the Greek letter pi (π) written above it in purple. At the bottom of the line is another black dot with the Greek letter pi prime (π') written below it in purple. The line segment itself is labeled with the letter 'e' in orange to its right.

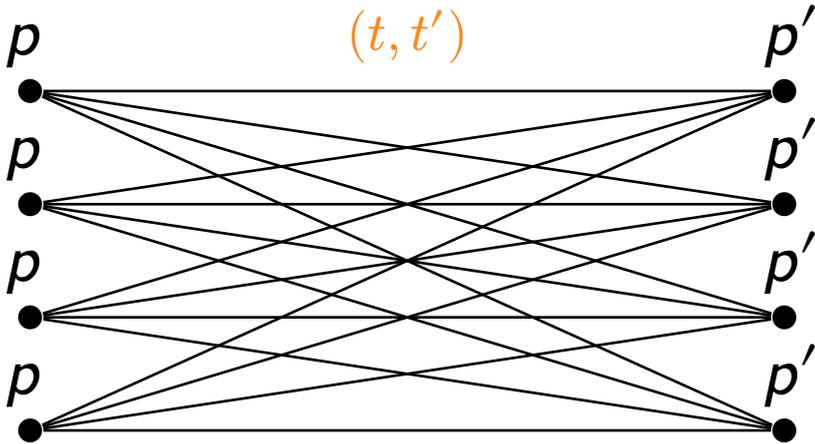
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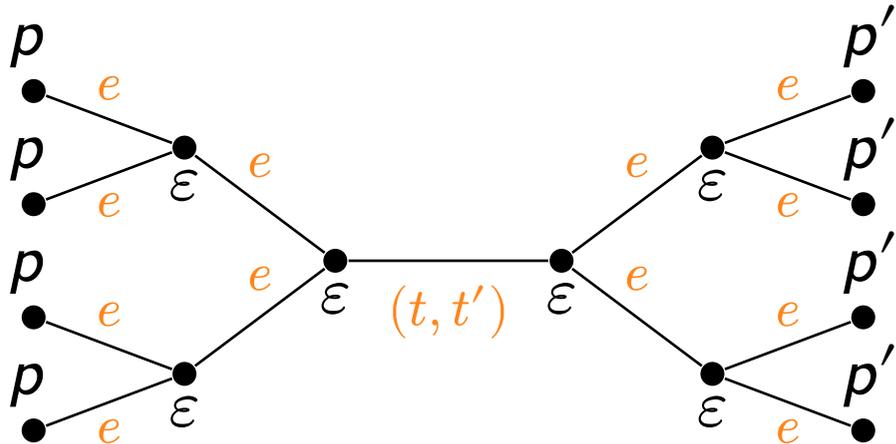
VR: All-pairs edges

$$\text{add}_{\pi, \pi'}^e \left(\begin{array}{ccc} \pi & & \pi \\ \bullet & & \bullet \\ & & \\ & \bullet & \bullet \\ & \pi' & \pi' \end{array} \right) = \left(\begin{array}{ccc} \pi & \pi & \pi \\ \bullet & \bullet & \bullet \\ & & \\ & \bullet & \bullet \\ & \pi' & \pi' \end{array} \right) e$$

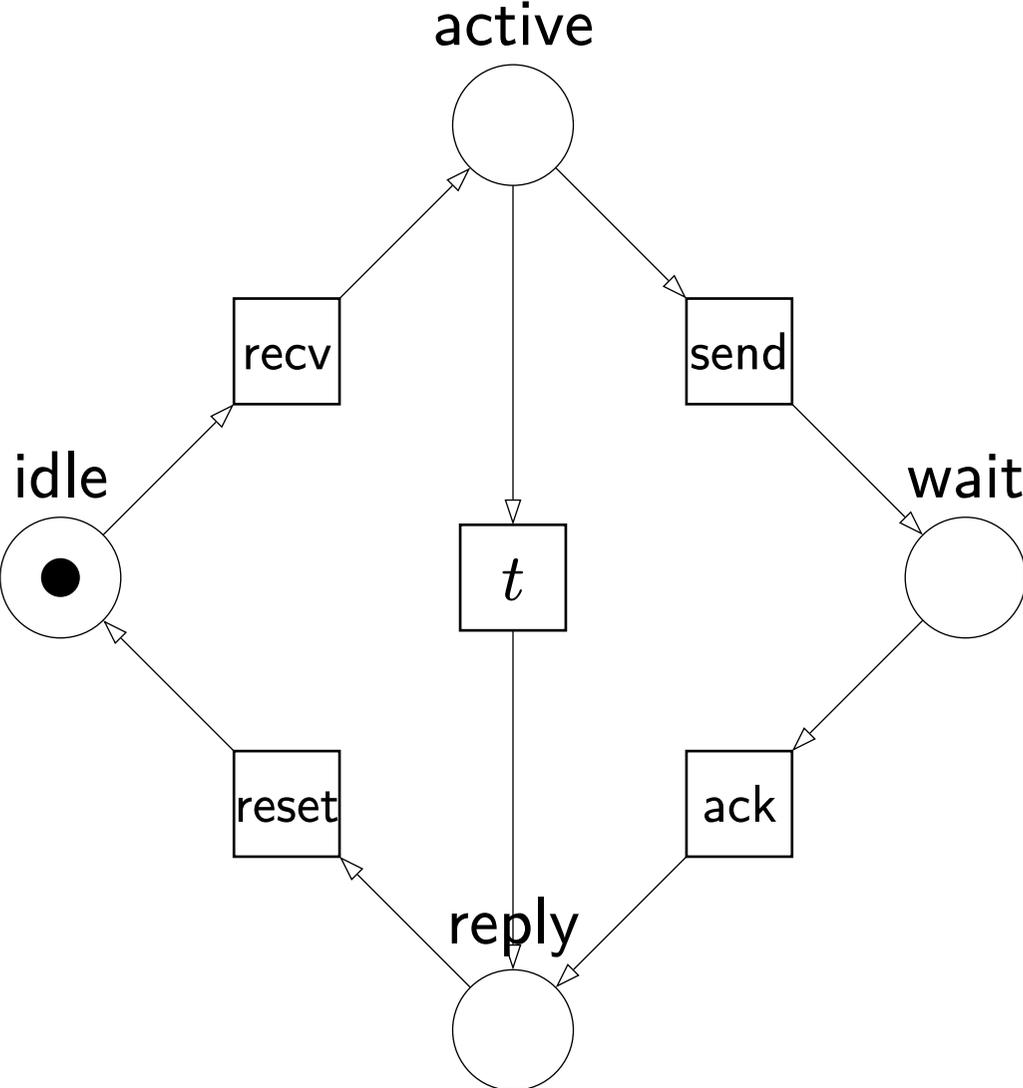
VR

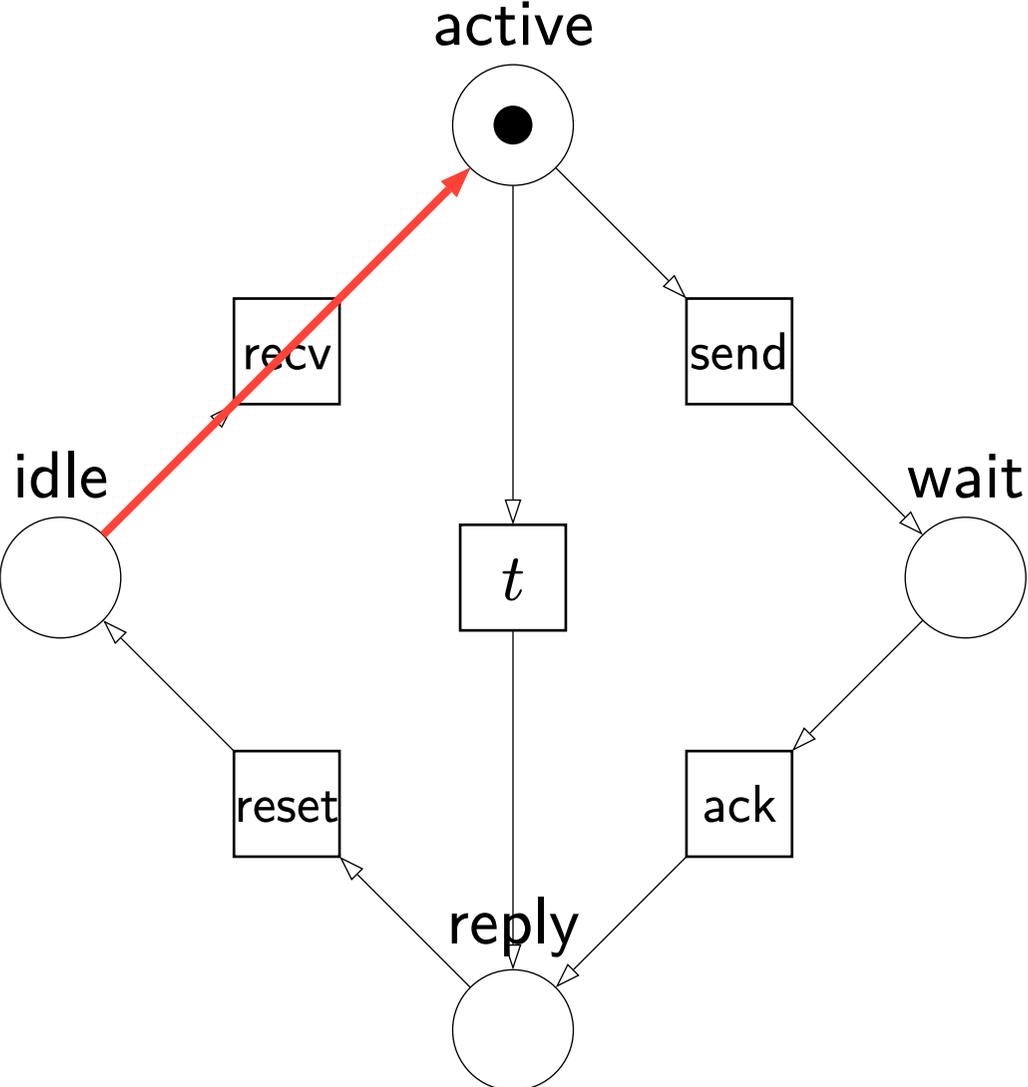


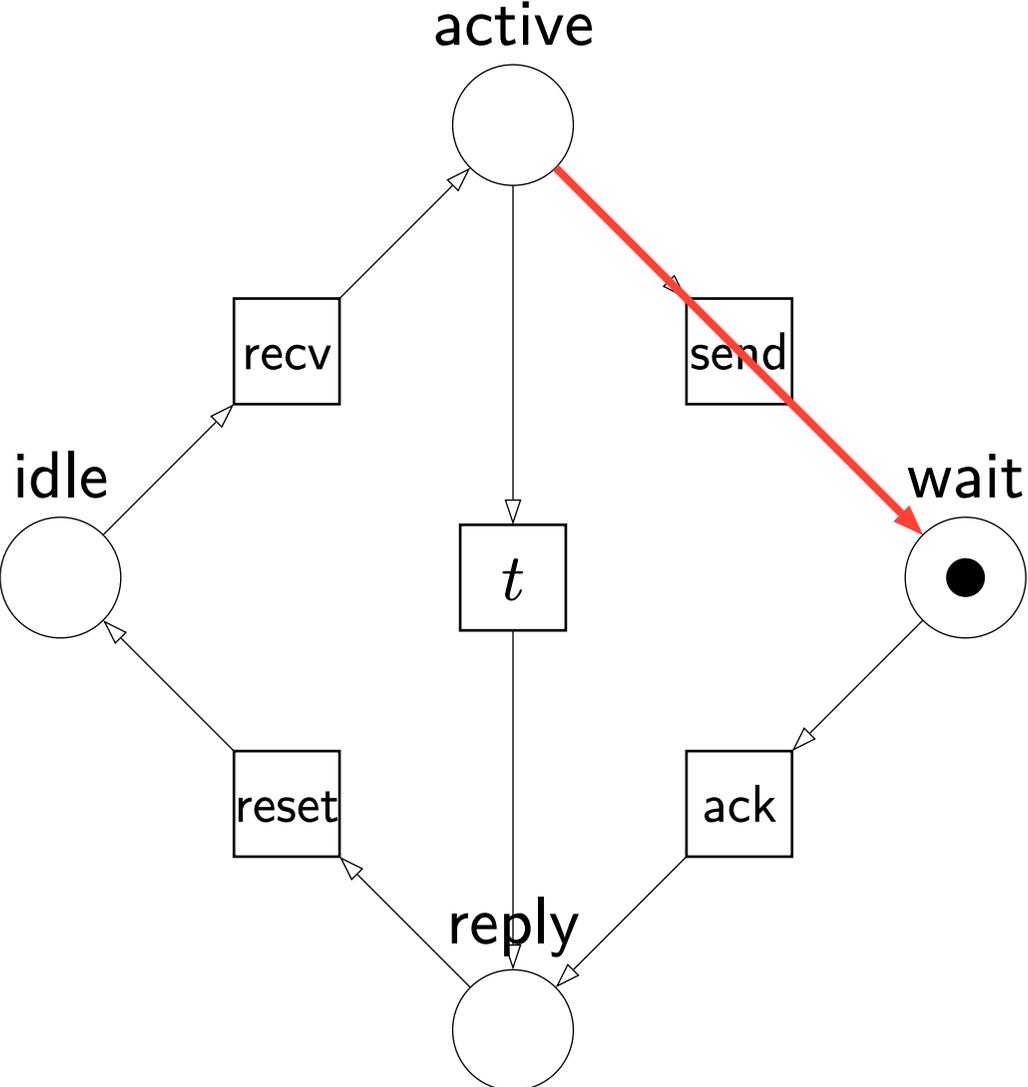
HR

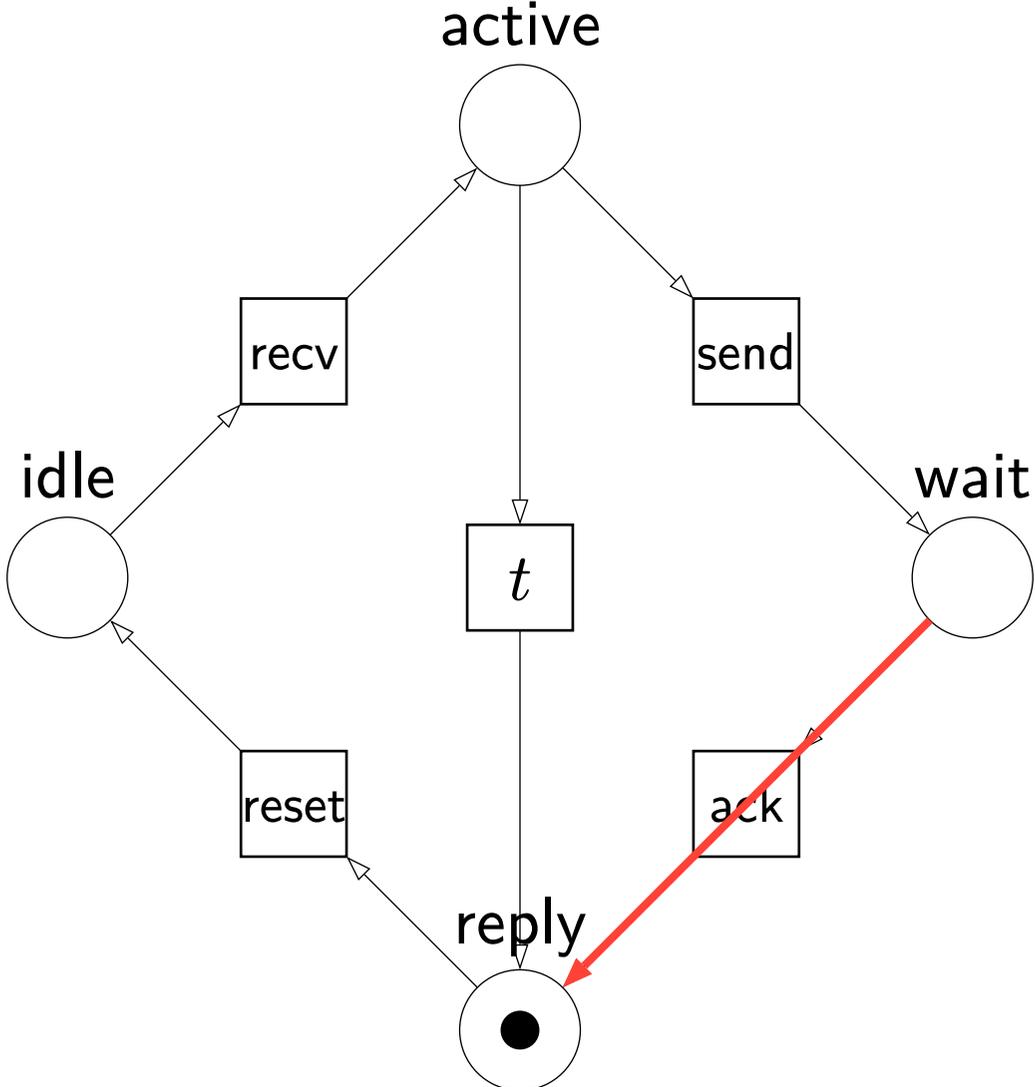


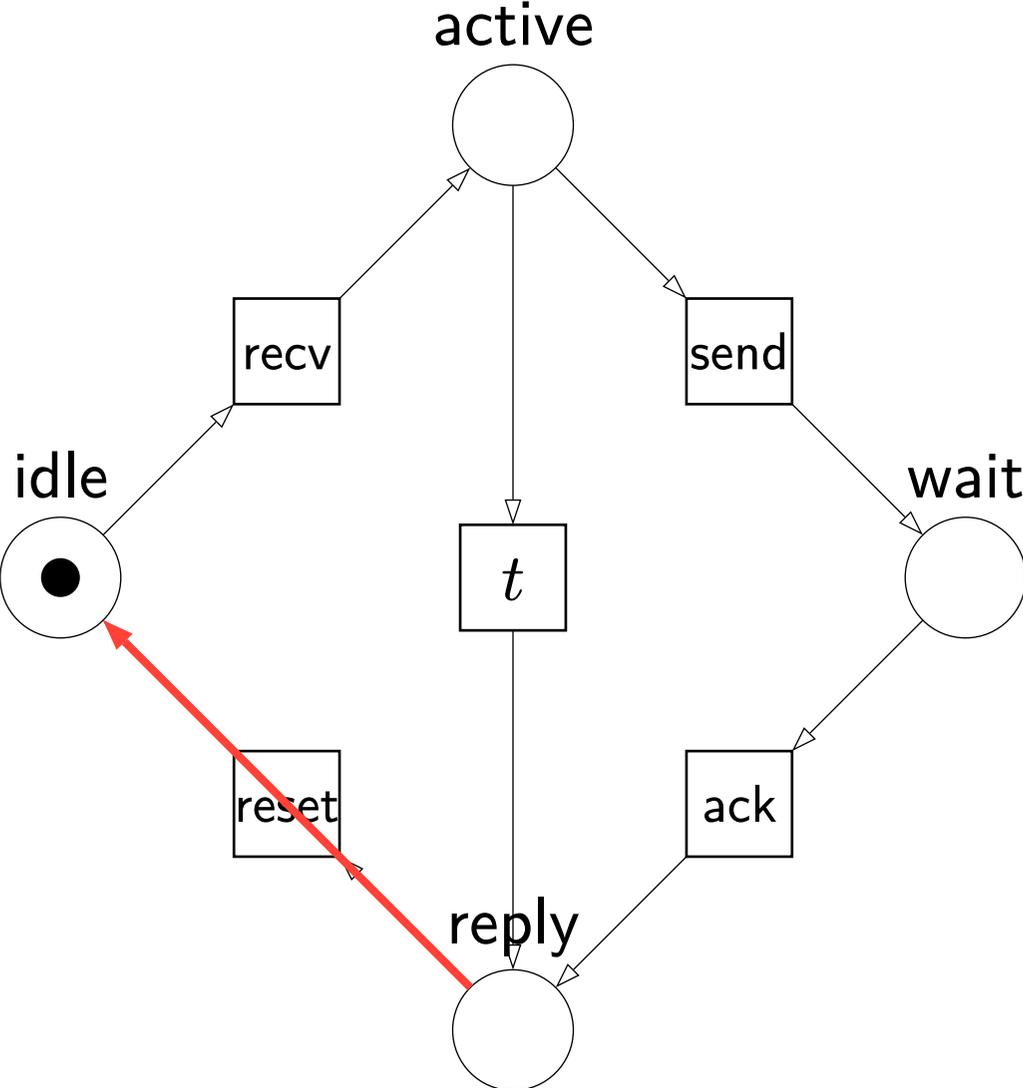
Routing

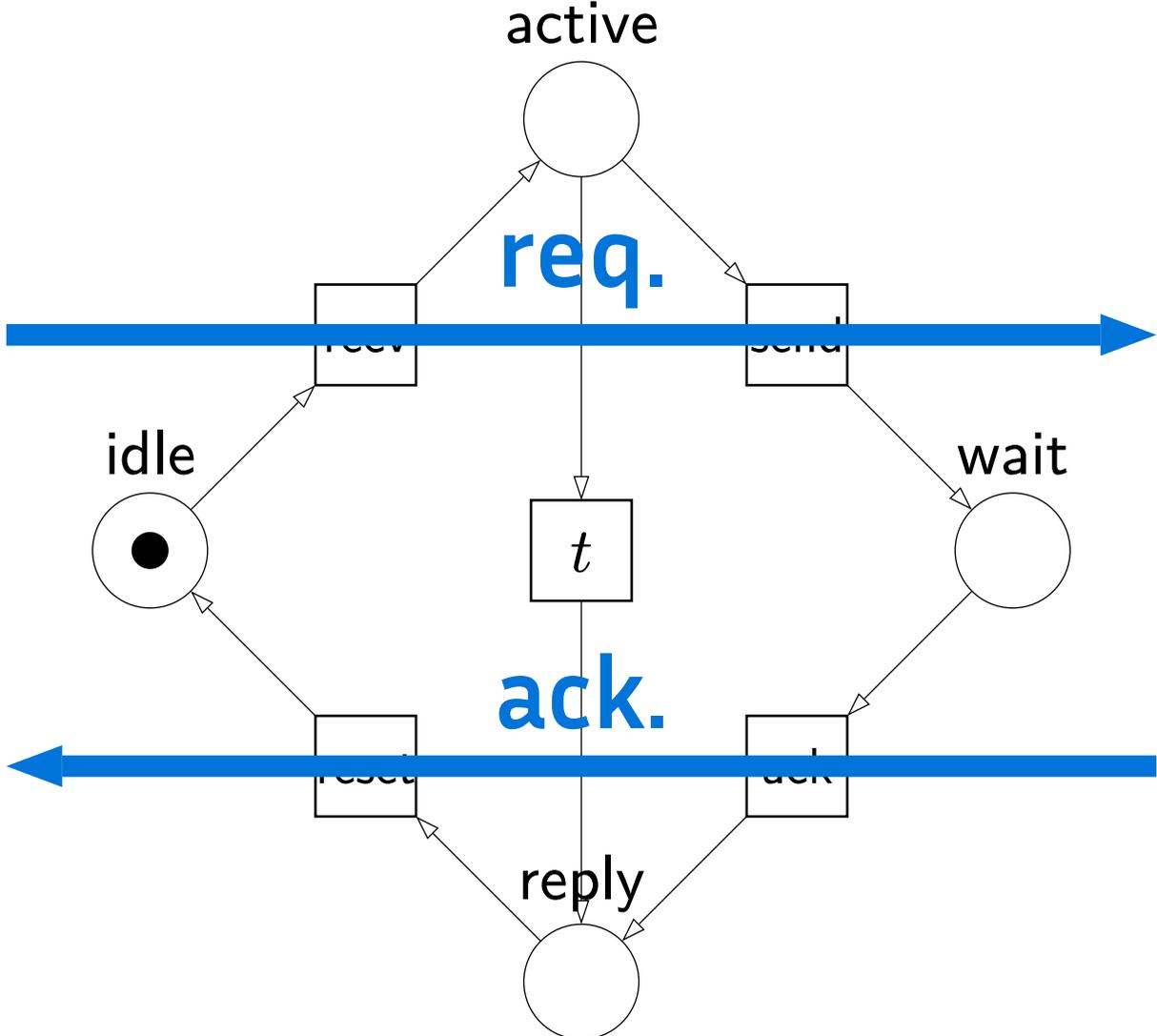




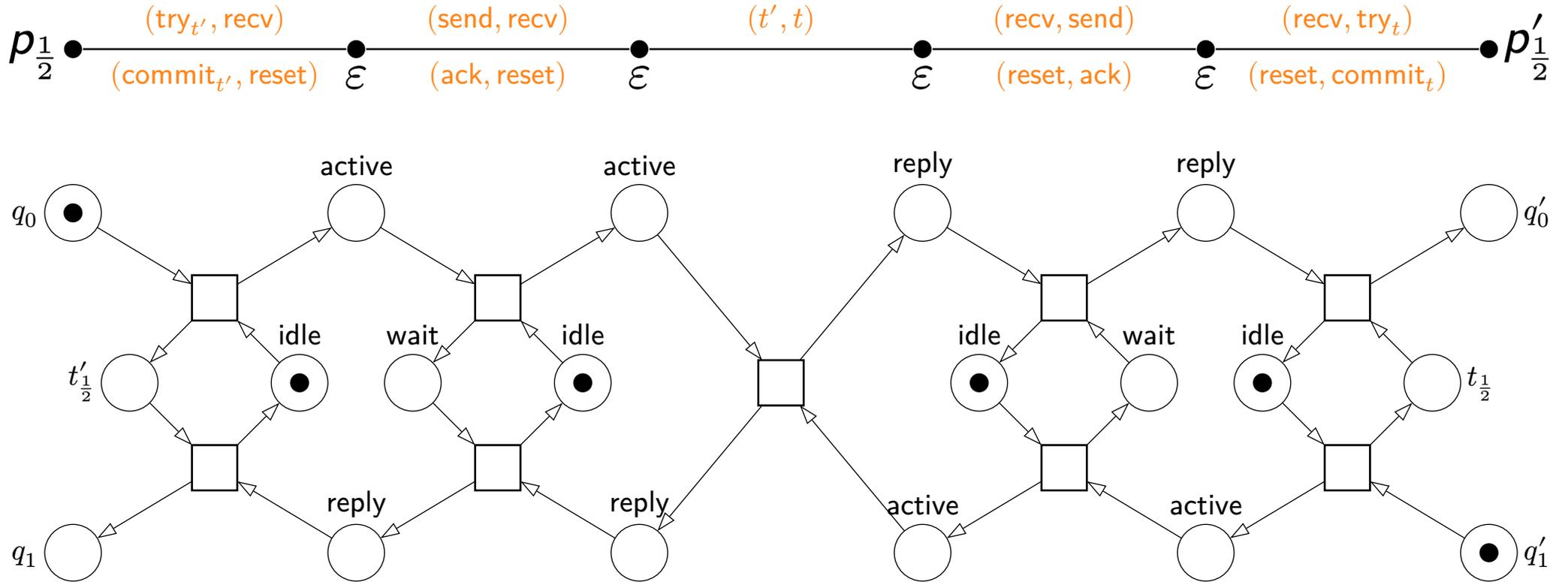




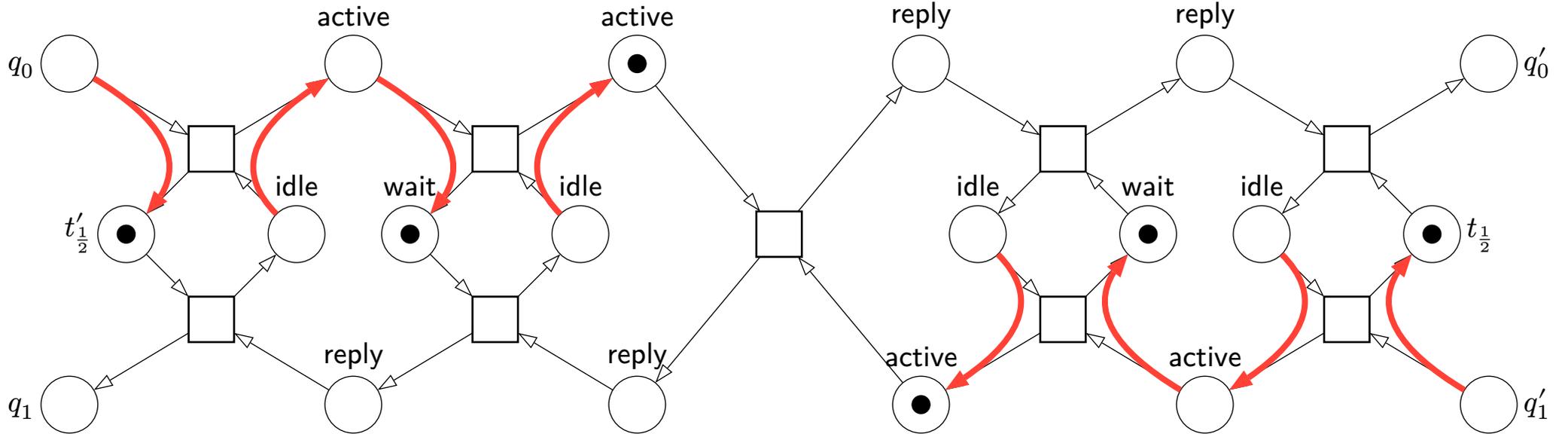
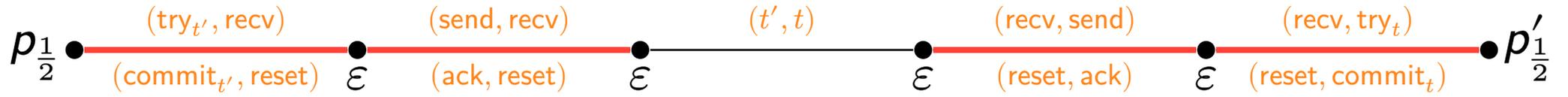




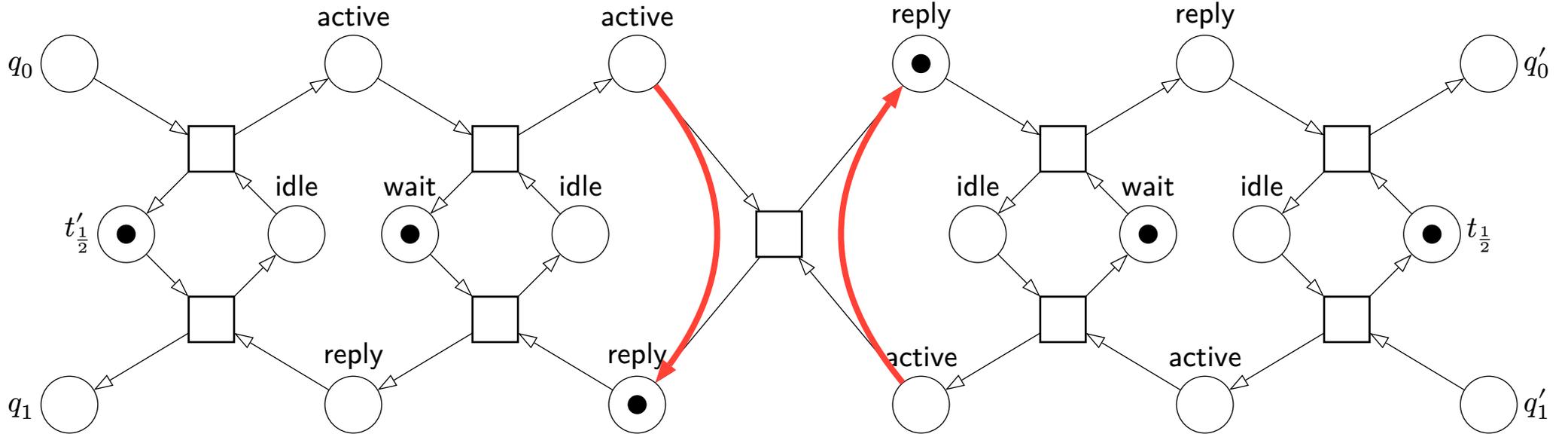
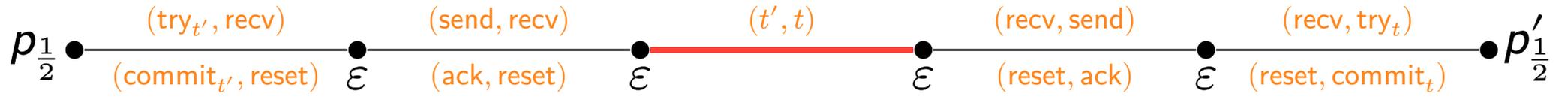
Communication through routers



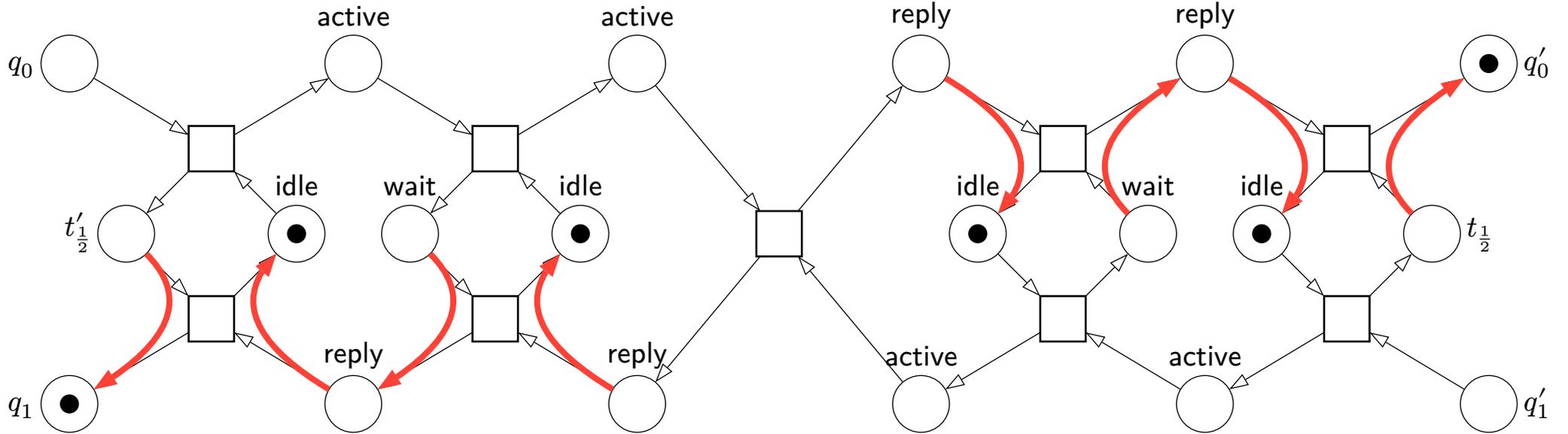
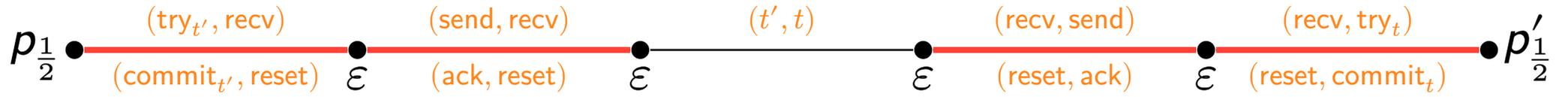
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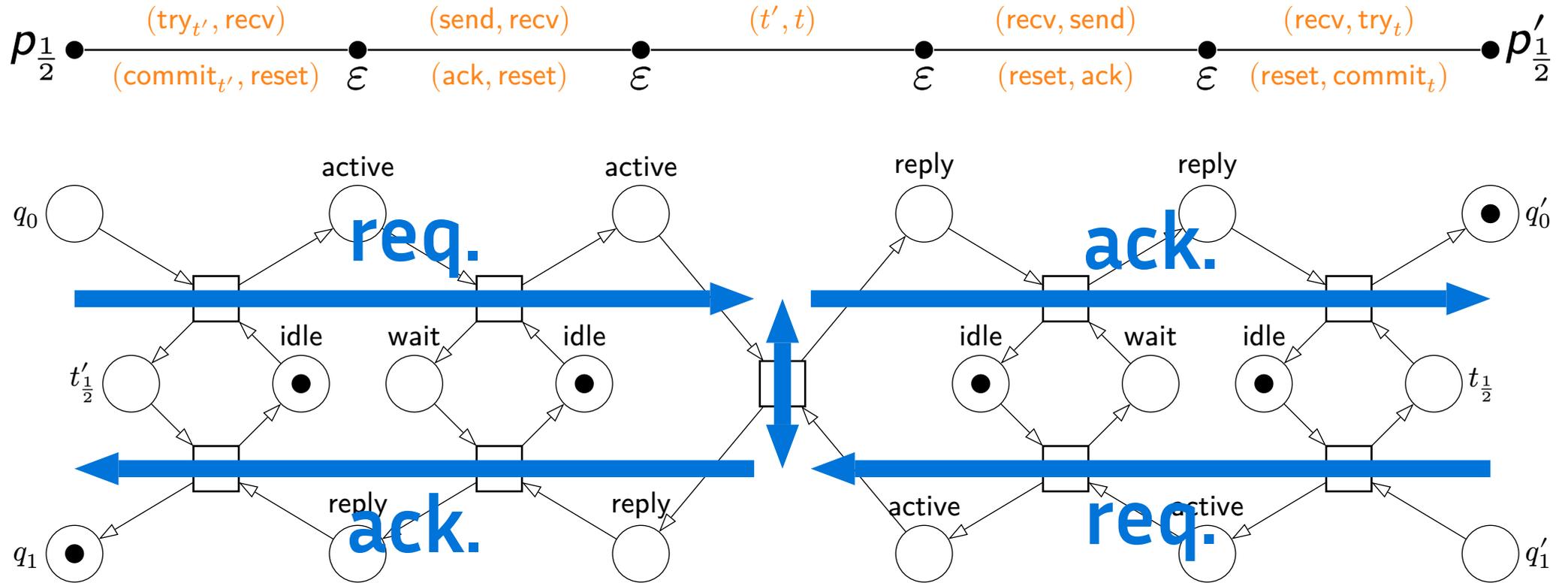
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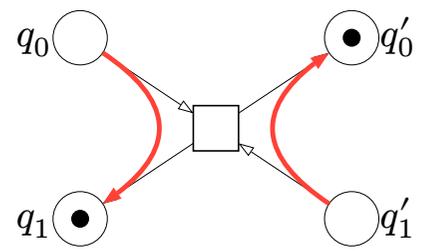


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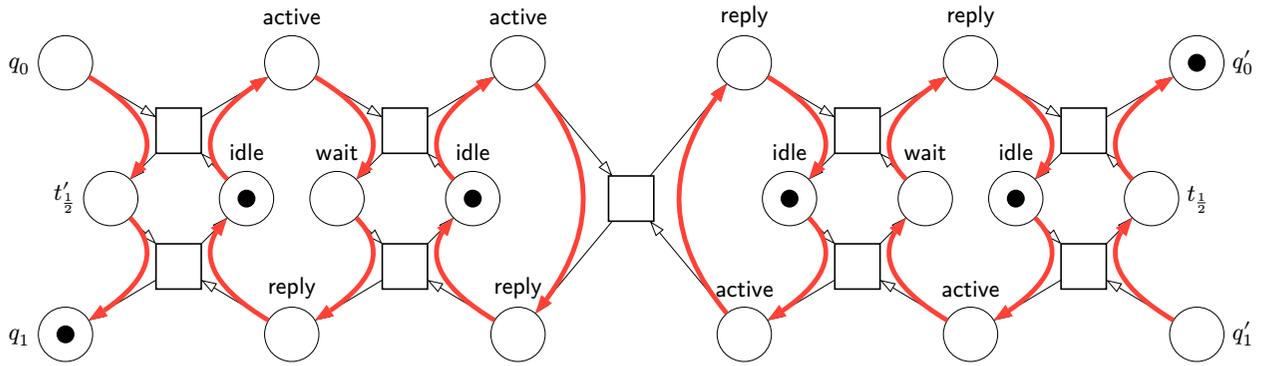
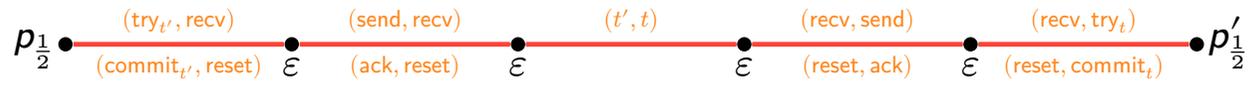


Stuttering

Routing



$s_1 s_2$



$s_1 s_1 s_1 s_1 s_1 s_2 s_2 s_2 s_2 s_2$

Simulation

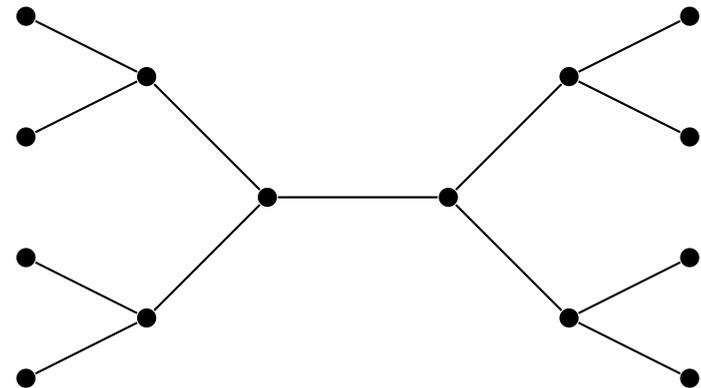
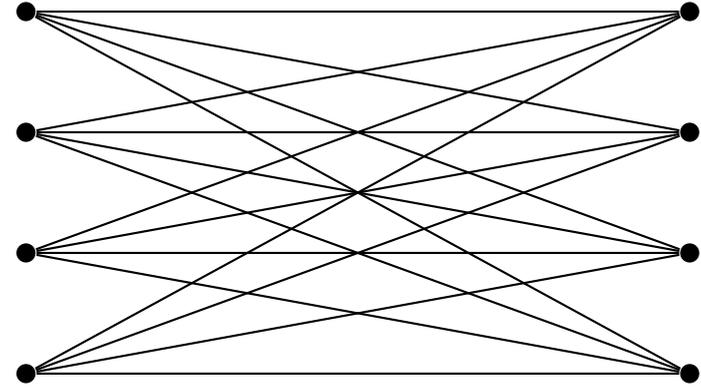
- Stuttering-invariant properties are preserved
 - (un)reachability, (un)coverability
 - mutual exclusion
 - reachability in a specific order
- Linear transformation
 - $|T| \cdot cw \cdot \Theta(n)$ router nodes
 - sparse graph

Downsides

- Lose properties sensitive to stuttering
 - ~~next-step~~ ($s_1 s_2$ vs $s_1 s_1 s_1 s_1 s_1 s_2$)
 - ~~deadlock~~ ($s_1 \perp$ vs $s_1 s_1 s_1 s_1 \perp$)
 - related: LTL $\setminus X$

- Increased trace length
 - $\times \Theta(n)$ worst-case
 - $\times \Theta(\lg n)$ average-case

- Loss of parallelism
 - finite throughput



Translation

Invariants

Translation

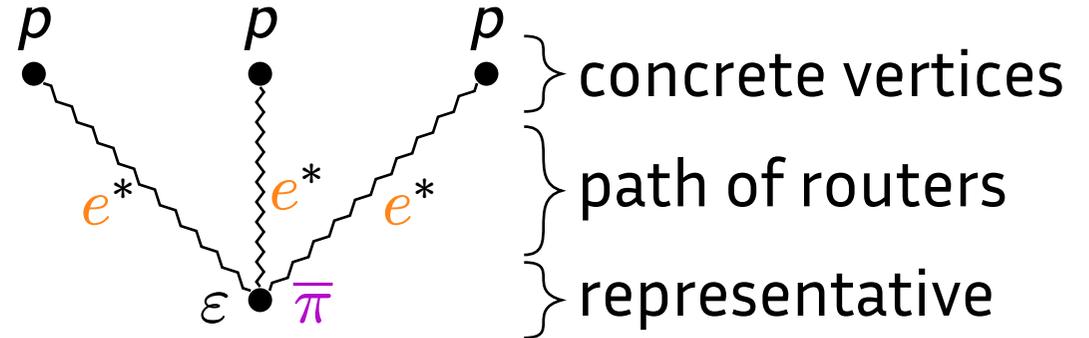
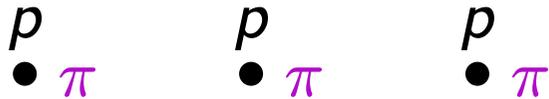
VR

HR

(t, t')
→

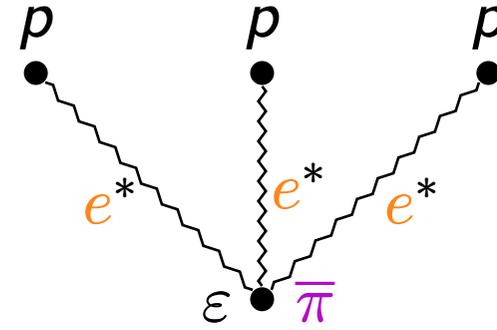
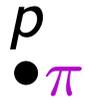
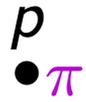
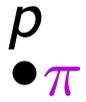
$e^* (t, t') e^*$
↔

H
→

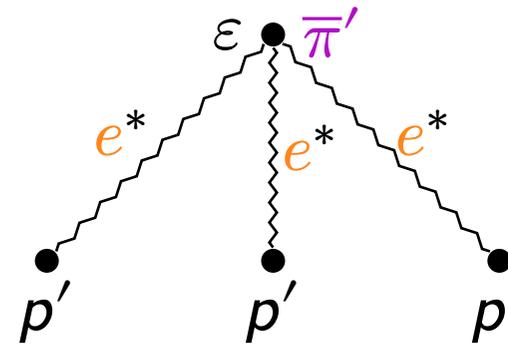


Edge creation

Translation



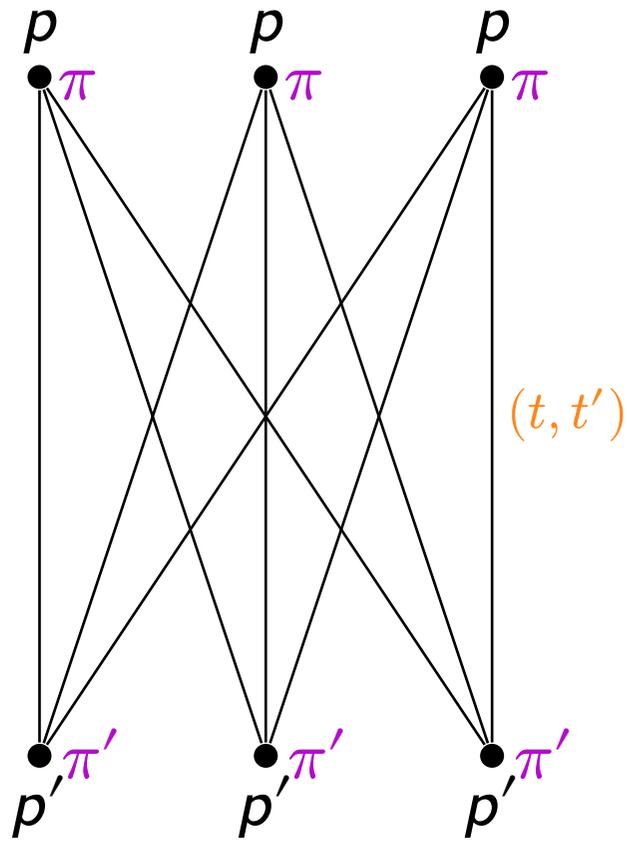
θ



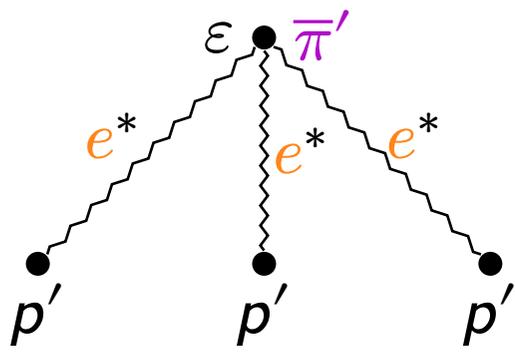
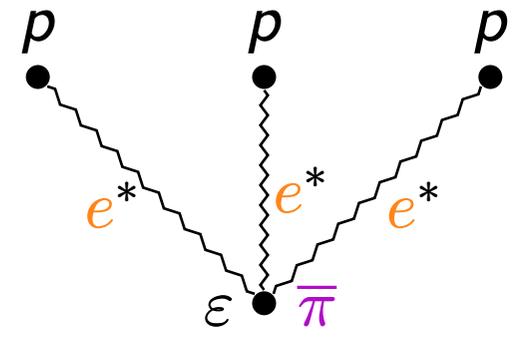
$H(\theta)$

Edge creation

Translation



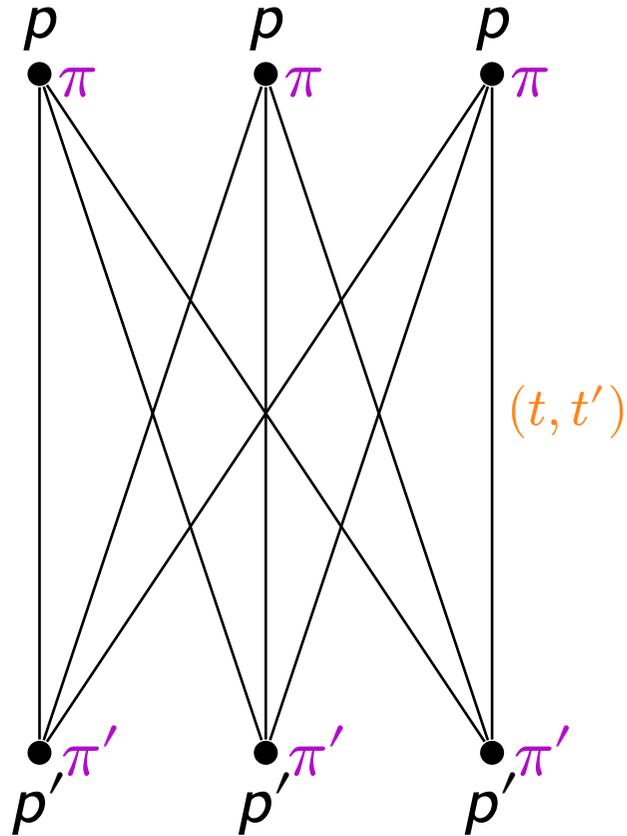
$\text{add}_{\pi, \pi'}^{(t, t')}(\theta)$



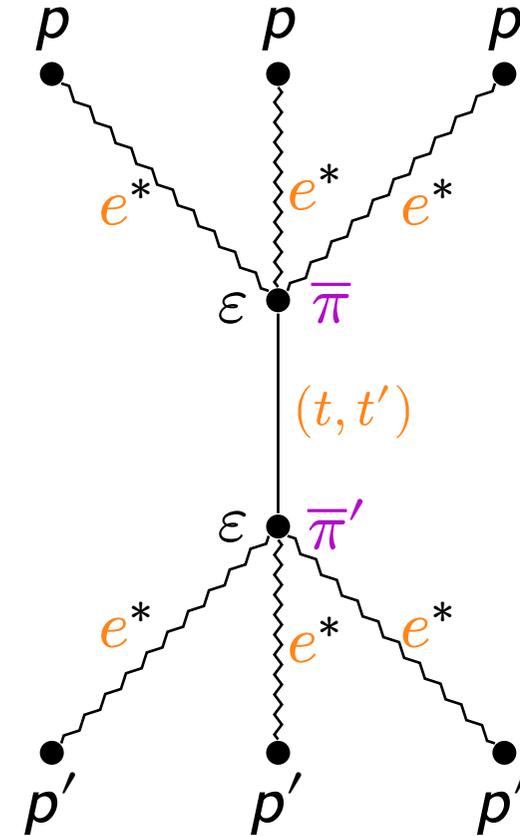
$H(\theta)$

Edge creation

Translation



$$\text{add}_{\pi, \pi'}^{(t, t')}(\theta)$$



$$H(\theta) \parallel \overrightarrow{(t, t')}_{\bar{\pi}, \bar{\pi}'}$$

Conclusion

- Translation of systems from **VR to HR**
- Preserves **stuttering-invariant** properties
- Enables applying semi-algorithms for HR to **dense families**